Low Power, High Precision Operational Amplifier

OP97

FEATURES

Low supply current: 600 µA maximum
OP07 type performance
Offset voltage: 20 µV maximum
Offset voltage drift: 0.6 µV/°C maximum
Very low bias current
25°C: 100 pA maximum
–55°C to +125°C: 250 pA maximum
High common-mode rejection: 114 dB minimum
Extended industrial temperature range: –40°C to +85°C

PIN CONNECTIONS

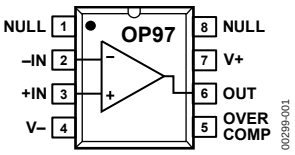


Figure 1. 8-Lead PDIP (P Suffix)
8-Lead SOIC (S Suffix)

GENERAL DESCRIPTION

The OP97 is a low power alternative to the industry-standard OP07 precision amplifier. The OP97 maintains the standards of performance set by the OP07 while utilizing only 600 µA supply current, less than 1/6 that of an OP07. Offset voltage is an ultralow 25 µV, and drift over temperature is below 0.6 µV/°C. External offset trimming is not required in the majority of circuits.

Improvements have been made over OP07 specifications in several areas. Notable is bias current, which remains below 250 pA over the full military temperature range. The OP97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power supply rejection are also improved with the OP97, at 114 dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from ±2.25 V to ±20 V, and the minimal power requirements of the OP97 combine to make the OP97 a preferred device for portable and battery-powered instruments.

The OP97 conforms to the OP07 pinout, with the null potentiometer connected between Pin 1 and Pin 8 with the wiper to V+. The OP97 upgrades circuit designs using AD725, OP05, OP07, OP12, and PM1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

			OP97E			OP97F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS									
Input Offset Voltage	V_{OS}			10	25		30	75	µV
Long-Term Offset Voltage Stability	ΔV_{OS}/Time			0.3			0.3		µV/month
Input Offset Current	I_{OS}			30	100		30	150	pA
Input Bias Current	I_B			±30	±100		±30	±150	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[1]		17	30		17	30	nV/√Hz
		f_O = 1000 Hz[2]		14	22		14	22	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		20			20		fA/√Hz
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V; R_L = 2 kΩ	300	2000		200	2000		V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5 V	114	132		110	132		dB
Input Voltage Range[3]	IVR		±13.5	±14.0		±13.5	±14.0		V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		V
Differential Input Resistance[4]	R_{IN}		30			30			MΩ
POWER SUPPLY									
Power Supply Rejection	PSR	V_S = ±2 V to ±20 V	114	132		110	132		dB
Supply Current	I_{SY}			380	600		380	600	µA
Supply Voltage	V_S	Operating range	±2	±15	±20	±2	±15	±20	V
DYNAMIC PERFORMANCE									
Slew Rate	SR		0.1	0.2		0.1	0.2		V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = 1	0.4	0.9		0.4	0.9		MHz

[1] 10 Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
[2] Sample tested.
[3] Guaranteed by CMR test.
[4] Guaranteed by design.

V_S = ±15 V, V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C for the OP97E/OP97F, unless otherwise noted.

Table 2.

			OP97E			OP97F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{OS}			25	60		60	200	µV
Average Temperature	TCV_{OS}	S suffix		0.2	0.6		0.3	2.0	µV/°C
Coefficient of V_{OS}							0.3		
Input Offset Current	I_{OS}			60	250		80	750	pA
Average Temperature	TCI_{OS}			0.4	2.5		0.6	7.5	pA/°C
Coefficient of I_{OS}									
Input Bias Current	I_B			±60	±250		±80	±750	pA
Average Temperature									
Coefficient of I_B	TCI_B			0.4	2.5		0.6	7.5	pA/°C
Large Signal Voltage Gain	A_{VO}	V_O = 10 V; R_L = 2 kΩ	200	1000		150	1000		V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5 V	108	128		108	128		dB
Power Supply Rejection	PSR	V_S = ±2.5 V to ±20 V	108	126		108	128		dB
Input Voltage Range[1]	IVR		±13.5	±14.0		±13.5	±14.0		V
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		V
Slew Rate	SR		0.05	0.15		0.05	0.15		V/µs
Supply Current	I_{SY}			400	800		400	800	µA
Supply Voltage	V_S	Operating range	±2.5	±15	±20	±2.5	±15	±20	V

[1] Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	±20 V
Input Voltage[1]	±20 V
Differential Input Voltage[2]	±1 V
Differential Input Current[2]	±10 mA
Output Short-Circuit Duration	Indefinite
Operating Temperature Range OP97E, OP97F (P, S)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.

[2] The inputs of the OP97 are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1 V cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

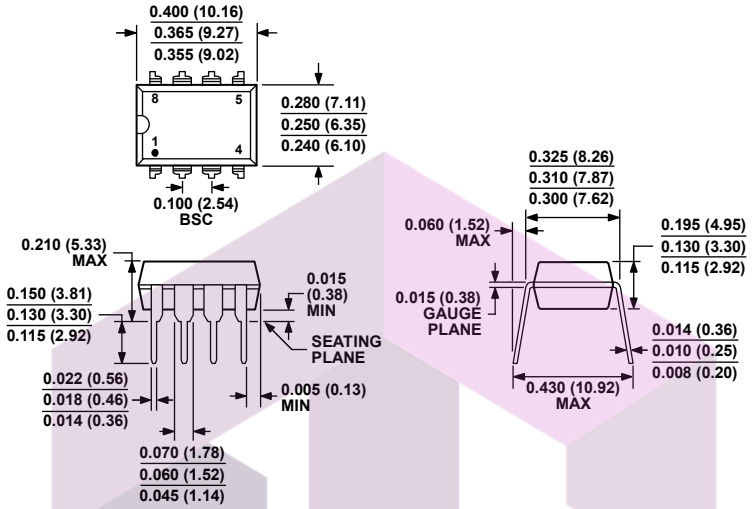
Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead PDIP (P Suffix)	103	43	°C/W
8-Lead SOIC (S Suffix)	158	43	°C/W

[1] θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for PDIP package; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

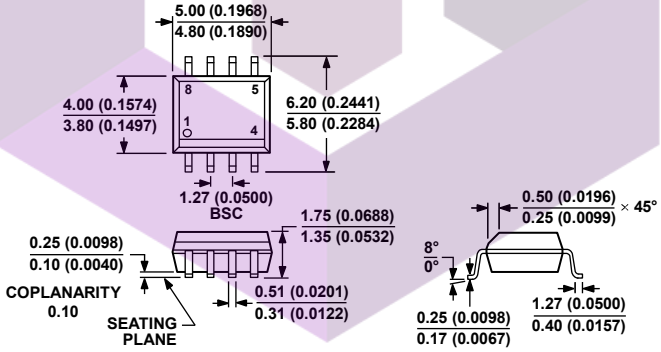
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 41. 8-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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Figure 42. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body
S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP97EP	−40°C to +85°C	8-Lead PDIP	N-8
OP97EPZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
OP97FP	−40°C to +85°C	8-Lead PDIP	N-8
OP97FPZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
OP97FS	−40°C to +85°C	8-Lead SOIC	R-8
OP97FS-REEL	−40°C to +85°C	8-Lead SOIC	R-8
OP97FS-REEL7	−40°C to +85°C	8-Lead SOIC	R-8
OP97FSZ[1]	−40°C to +85°C	8-Lead SOIC	R-8
OP97FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	R-8
OP97FSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	R-8

[1] Z = RoHS Compliant Part.